NON-VOLATILE MEMORY ERASE CIRCUITRY

ABSTRACT OF THE DISCLOSURE

A non-volatile memory device includes floating gate memory cells, a pulse counter and voltage pump control circuitry. The control circuitry selectively activates pumps in response to a count output of the counter. In one embodiment, the pump output current is increased as the counter output increases. The memory allows for erase operations that reduce leakage current during initiation of an erase operation.